Improved Multiple Block Adder Using Carry Increment Adder

[0001] The present application claims priority from U.S. Provisional Application serial no. 60/269,450 filed December 22,2000, entitled "A Low Power and High Performance Multiply Accumulate (MAC) Module" of Kaoru Awaka et al. This disclosure is incorporated herein by reference.

Field of Invention:

[0002] This invention relates to an improved adder architecture in which both a carry increment adder is used with a carry lookahead adder.

Background of Invention:

[0003] A conventional N-bit comprises adder building blocks. A common adder building block is a full adder that takes as inputs bit A, bit B and carry-in bit Cin and produces sum S and carry-out Cout as illustrated in Figure 1. A cascade of N full adders can be used to provide an N-bit ripple carry adder as illustrated in Figure 2. Figure 2 illustrates three adders adding three bits at input A (bits 0-2) to three bits at input B (bits 0-2) to get sum bits S0-S2) and carry (Cout). A ripple carry adder is one that the output sum gets updated from lower bits. The higher bit waits for the carry propagation from the lower bit adder. A ripple carry adder is too slow for most long adders since an n bit ripple carry takes N full delays.

[0004] The delay can be reduced by carry lookahead adder (CLA) that computes the carry through several bits using one complicated gate instead of a cascade of several full adders. An example of a 16-bit lookahead adder is illustrated in Fig. 3. It has four 4-